REMARKS

Favorable reconsideration of this application as amended is respectfully requested. Claims 2, 3, 7, 9,14, 34, and 35 were amended so as to overcome the objections of the Examiner. Additionally, in claim 14, line 7, the word "mechanically" has been replaced with "electrically". Support for this change can be found, for example, at page 2, lines 1-3. A Letter to the Master Draftsman accompanies this amendment with corrections to the drawings. No new matter has been introduced.

DRAWINGS

The drawings have been objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include the following reference sign mentioned in the description: page 7, line 6 of the specification refers to a planarizing dielectric material "550". In Fig. 5, the reference number "550" has been added to indicate the planarizing dielectric material. A Letter to the Master Draftsman accompanies this amendment with the correction to the drawing.

The drawings were also objected to as failing to comply with 37 C.F.R. 1.84(p)(4) because reference character "520" on page 7, line 3 of the specification has been used to designate both bare die and device. On page 7, line 1, reference number "520" is introduced as "a bare die planar electronic device 520". The following changes to the specification have been made for consistency: at page 7, line 3, the words "bare die" have been replaced with --device--; at page 7, line 5 the words "bare die" have been replaced with --device--; and on page 7, line 8, the words "bare die" have been replaced with the words "device".

35 U.S.C. §102(a)

Claims 1-3, 5-22, and 32-36 stand rejected under 35 U.S.C. §102(e) as being anticipated by Wyland (5,986,885). Claim 1 reads:

1. An electronic component comprising:

a silicon package having a recess, the recess including a conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

In contrast to claim 1, Wyland discloses a bare die 30 having a plurality of die bonding pads 31 located on the *top surface* of the bare die 30 (see Wyland at Fig. 1), but not a non-top terminal as required by claim 1. A non-top terminal is neither taught nor suggested in Wyland.

Furthermore, while a sponge 40 is thermally coupled to the bottom surface of the die 30 in Wyland, the sponge 40 acts as an internal heatsink (see Wyland at col. 5, lines 51-54). No terminal, much less a non-top terminal, is *electrically* coupled to the sponge 40 in Wyland. A non-top terminal electrically coupled to the conductive region, as required in claim 1, is neither taught nor suggested in Wyland.

Additionally, Wyland does not disclose a *silicon* package having a recess in which a bare die electronic device is disposed, as required by claim 1. Instead, in fig. 1 of Wyland, a bare die 30 is coupled to a die attach paddle 25 which is typically made of thermal conductive material such as copper (see Wyland at col. 1, lines 30-40). The die attach paddle 25 is further coupled to a thermally conductive metal sponge 40 (see Wyland at col. 5, lines 49-55). An encapsulant 45 is then applied over the entire assembly (see Wyland at col. 6, lines 5-10). Accordingly, fig.1 in Wyland does not disclose the use of silicon as a packaging material, nor does it disclose a package having a recess. A silicon package having a recess in which a bare die electronic device is disposed is neither taught nor suggested in Wyland.

Since Wyland does not teach every element of claim 1, claim 1 is not anticipated under 35 U.S.C. §102(e) by Wyland. Claims 2, 3, and 5-13 depend on independent claim 1 and are allowable for the same reasons.

Independent claim 14 requires an electronic component that includes a non-top terminal electrically coupled to the conductive region. As discussed above, a non-top terminal electrically coupled to the conductive region is neither taught nor suggested in Wyland. Accordingly, claim 14 is not anticipated under 35 U.S.C. §102(e) by Wyland.

Claim 15 depends on independent claim 14 and is allowable for the same reason as claim 14.

Independent Claim 16 teaches the same elements and limitations of claim 1 that distinguish the claim over Wyland and is therefore allowable for the same reasons as claim 1. Claims 17-20 depend on independent claim 16 and are allowable for the same reasons as claim 1.

Independent claim 21 requires an electronic component that includes a first terminal and a second terminal, wherein a first dimension is defined therebetween. A silicon package has a first surface and a second surface, the silicon package having a recess on the first surface that has a depth that is substantially equal to the first dimension.

In contrast, a *silicon* package, as required by claim 21, is neither taught nor suggested in Wyland, as discussed above. Furthermore, Wyland discloses a package having a recess on the first surface that has a depth that is greater than the dimension between the packages two terminals (see Wyland at fig. 4). A package having a recess on the first surface that has a depth that is substantially equal to the first dimension, as required by claim 21, is neither taught nor suggested by Wyland. Accordingly, claim 21 is not anticipated under 35 U.S.C. §102(e) by Wyland. Claim 22 depends on independent claim 21 and is allowable for the same reasons as claim 21.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, the semiconductor package in Fig. 1 of Wyland does not show a package having a recess, as discussed above with respect to claim 1. Furthermore, the encapsulant used in fig. 1 of Wyland covers the entire assembly, including the bonding wires (see Wyland at col. 6, lines 5-15), and does not create a level plane that includes the top of the device. as required by claim 1. Planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Wyland. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(e) by Wyland. Claims 33-36 depends on independent

claim 32 and are allowable for the same reasons as claim 32. Thus, claims 1-3, 5-22, and 32-36 are patentable over Wyland.

Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. §102(e) as being anticipated by Suzuki et al. (5,977,633). Claim 1 requires an electronic component that includes a silicon package having a recess. The recess includes a conductive region. A bare die electronic device having a non-top terminal is disposed in the recess. The non-top terminal is electrically coupled to the conductive region.

In contrast, Suzuki discloses a package that includes a *metal base substrate* having a recess (see Suzuki at fig. 1, and col. 4, lines 18-34), as opposed to a *silicon* package having a recess as required by claim 1. A silicon package having a recess is neither taught nor suggested by Suzuki. Accordingly, claim 1 is not anticipated under 35 U.S.C. §102(e) by Suzuki.

Independent claim 14 requires a package having a recess. A bare die electronic device is disposed in the recess. The bare die electronic device includes both a non-top terminal and a top terminal.

In contrast, Suzuki discloses a bare die electronic device that includes a plurality of top terminals (for example, see Suzuki at fig. 1). A bare die electronic device that includes a non-top terminal and a top terminal is neither taught nor suggested in Suzuki. Accordingly, claim 14 is not anticipated under 35 U.S.C. §102(e) by Suzuki.

Independent claims 16 and 21 teach the same elements and limitations of claim 1 that distinguish the claim over Suzuki and are therefore allowable for the same reasons as claim 1.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, Suzuki discloses a package that includes a bare die electronic device disposed in a recess, wherein seal resin is used to fill the entire recess, including the bonding wires (see Suzuki at fig. 1 and col. 4, lines 55-58). Hence, the seal resin does not create a level plane that includes the top of the device, as required by claim 32. Planarizing material filling the recess not occupied by the device to substantially create a

level plane that includes the top of the device is neither taught nor suggested by Suzuki. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(e) by Suzuki. Thus, claims 1, 14, 16, 21, and 32 are patentable over Suzuki.

Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. §102(b) as being anticipated by Andros et al. (5,633,533). Claim 1 requires an electronic component that includes a silicon package having a recess. The recess includes a conductive region. A bare die electronic device having a non-top terminal is disposed in the recess. The non-top terminal is electrically coupled to the conductive region.

In contrast, Andros discloses a chip 41 having a plurality of electrical contact sites located on surface 45 of the chip 41 (see Andros at fig. 4 and col. 4, line 62 to col. 5, line 9., but not a non-top terminal as required by claim 1. A non-top terminal is neither taught nor suggested in Andros.

Furthermore, Andros discloses a package that includes a *thermally conductive* support member 31 having an indentation 33 (see Andros at col. 4, lines 26-28). The support member 31 is preferably a *metal* such as copper (see Andros at col. 4, lines 30-32), and is not a silicon package as required by claim 1. A silicon package having a recess is neither taught nor suggested by Andros. Since Andros does not teach every element of claim 1, claim 1 is not anticipated under 35 U.S.C. §102(b) by Andros.

Independent claim 14 requires a package having a recess. A bare die electronic device is disposed in the recess. The bare die electronic device includes both a non-top terminal and a top terminal.

In contrast, Andros discloses a chip 41 that includes a plurality of electrical contact sites located on the top surface 45 of chip 41 (see Andros at fig. 4 and col. 4, line 62 to col. 5, line 9). The chip 41 does not have both a top terminal and a non-top terminal as required by claim 14. Furthermore, a bare die electronic device that includes a non-top terminal and a top terminal is neither taught nor suggested in Andros. Accordingly, claim 14 is not anticipated under 35 U.S.C. §102(b) by Andros.

Independent claims 16 and 21 teach the same elements and limitations of claim 1 that distinguish the claim over Andros and are therefore allowable for the same reasons as claim 1.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, Andros discloses a package that includes a chip 41 disposed in a recess 33, wherein encapsulant 51 is added to cover the external surface 45 of the chip 41, as well as the bonding wires 49 and portions of adjacent circuitry 17 (see Andros at fig. 5 and col. 5, lines 20-33). Hence, the encapsulent does not create a level plane that includes the top of the device, as required by claim 32. Planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Andros. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(b) by Andros. Thus, claims 1, 14, 16, 21, and 32 are patentable over Andros.

Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. §102(b) as being anticipated by Corisis (5,633,533). As a preliminary matter, it should be noted that Corisis is not prior art under 35 U.S.C. §102(b).

Claim 1 requires an electronic component that includes a silicon package having a recess. The recess includes a conductive region. A bare die electronic device having a non-top terminal is disposed in the recess. The non-top terminal is electrically coupled to the conductive region.

In contrast, Corisis discloses a semiconductor assembly that includes a semiconductor device 100 that is supported by a lead frame 10 (see Corisis at fig. 1 and accompanying text). The semiconductor device is encapsulated in an epoxy plastic material to form a package 200 (see Corisis at col. 4, lines 41-47). Hence, the semiconductor device 100 is not disposed in a recess of a silicon package, as required by claim 1. Furthermore, a silicon package having a recess is neither taught nor suggested by Corisis. Since Corisis does not teach every element of claim 1, claim 1 is not anticipated under 35 U.S.C. §102(b) by Corisis.

Independent claim 14 requires a package having a recess. A bare die electronic device is disposed in the recess. The bare die electronic device includes both a non-top terminal and a top terminal.

In contrast, Corisis discloses a semiconductor device 100 that includes a plurality of bond pads 102 on top active surface 108 (see Corisis at fig. 2 and col. 4, line 63 to col. 5, line 7). The semiconductor device 100 does not have both a top terminal and a non-top terminal as required by claim 14. Furthermore, a bare die electronic device that includes a non-top terminal and a top terminal is neither taught nor suggested in Corisis. Accordingly, claim 14 is not anticipated under 35 U.S.C. §102(b) by Corisis.

Independent claims 16 and 21 teach the same elements and limitations of claim 1 that distinguish the claim over Corisis and are therefore allowable for the same reasons as claim 1.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, Corisis discloses that after wire bonds 50 are connected, the entire device 100 is encapsulated in epoxy plastic material to form a package (see Corisis at fig. 2 and col. 4, lines 41-47). Hence, the encapsulent does not create a level plane that includes the top of the device, as required by claim 32. Planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Corisis. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(b) by Corisis. Thus, claims 1, 14, 16, 21, and 32 are patentable over Corisis.

Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. §102(b) as being anticipated by Hernandez et al (hereinafter Hernandez) (5,095,402). Claim 1 requires an electronic component that includes a silicon package having a recess. The recess includes a conductive region. A bare die electronic device having a non-top terminal is disposed in the recess. The non-top terminal is electrically coupled to the conductive region.

In contrast, Hernandez discloses a chip 38 that is supported by a lead frame 10 that is encapsulated in a molded package 44 (see Hernandez at col. 4, lines 32-33). Hence, the semiconductor device 100 is not disposed in a recess of a silicon package, as required by claim 1. Furthermore, a silicon package having a recess is neither taught nor

suggested by Hernandez. Since Hernandez does not teach every element of claim 1, claim 1 is not anticipated under 35 U.S.C. §102(b) by Hernandez.

Independent claim 14 requires a package having a recess. A bare die electronic device is disposed in the recess. The bare die electronic device includes both a non-top terminal and a top terminal.

In contrast, Hernandez discloses a plurality of bond pads 114, 116 on the top surface of the die (see Hernandez at col. 7, lines 7-24). Hence, the die does not have both a top terminal and a non-top terminal as required by claim 14. Furthermore, a bare die electronic device that includes a non-top terminal and a top terminal is neither taught nor suggested in Hernandez. Accordingly, claim 14 is not anticipated under 35 U.S.C. §102(b) by Hernandez.

Independent claims 16 and 21 teach the same elements and limitations of claim 1 that distinguish the claim over Hernandez and are therefore allowable for the same reasons as claim 1.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, Hernandez discloses that the chip 38, wire bonds 40, decoupling capacitor, and lead frame 10 are encapsulated to form a molded package 44 (see Hernandez at fig. 3a and col. 4, line 32-33). Hence, an encapsulent does not create a level plane that includes the top of the chip (device), as required by claim 32. Planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Hernandez. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(b) by Hernandez. Thus, claims 1, 14, 16, 21, and 32 are patentable over Hernandez.

Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. §102(b) as being anticipated by Hebert (4,649,415). Claim 1 requires an electronic component that includes a silicon package having a recess. The recess includes a conductive region. A bare die electronic device having a non-top terminal is disposed in the recess. The non-top terminal is electrically coupled to the conductive region.

In contrast, Hebert discloses a die 30 that is housed in a polymeric thermoplastic material, such as polyethersulfone, polyethyerimide, or polyphenylene sulfide. (see Hebert at col. 3, lines 16-24. Hence, the die 30 is not disposed in a recess of a silicon package, as required by claim 1. Furthermore, a silicon package having a recess is neither taught nor suggested by Hebert. Since Hebert does not teach every element of claim 1, claim 1 is not anticipated under 35 U.S.C. §102(b) by Hebert.

Independent claim 14 requires an electronic component that includes a package having a recess. The recess includes a first deposition-processed conductive region. A bare die electronic device is disposed in the recess. The bare die electronic device includes both a non-top terminal and a top terminal. The non-top terminal is electrically coupled to the conductive region, and the top terminal is electrically coupled to a second deposition-processed conductive region.

In contrast, Hebert discloses a semiconductor package that includes die terminals that are electrically coupled to conductive tape via wire bonding, unlike claim 14 which requires die terminals that are electrically coupled to deposition-processed conductive regions. In Hebert, bond pads 42 on die 30 are wire bonded 29 to conductive tape 20, which is further connected to contact fingers of a lead frame (see Hebert at fig. 5, and col. 2, line 47 to col. 3, line 3). Hence, the terminals 42 in Hebert are not electrically coupled to deposition-processed conductive regions as required by claim 14. Additionally, electrically coupling die terminals to a deposition-processed conductive regions is neither taught nor suggested in Hebert.

The Examiner has suggested in the subject office action that claim 14 includes product-by-process language, "deposition-processed conductive region." Even though product-by-process claims are limited and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in a product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art is made by a different process. *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). The electronic component of claim 14 is different, and non-obvious, over the semiconductor package in Hebert. For example, the deposition-processed conductive regions in claim 14 are more conducive to high frequency signals

than the wire bonding disclosed in Hebert, since at high frequencies the dimension of the wire becomes an issue. In particular, the cutting of the wire results in a less repeatable conductor length compared to a deposition-processed conductive region. Furthermore, Hebert does not teach or suggest electrically coupling the die terminals to a deposition-processed conductive region (see above). A suggestion or motivation to combine prior art references must appear in the prior art itself in order to establish obviousness to combine two references and may not be inferred in hindsight from the subsequent invention of the patentee. *In re Dance*, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998). In particular, without hindsight, electrically coupling terminal 42 to a deposition-processed conductive region in Hebert would be problematical due to the gap between die 30 and interior ledge 12a. Accordingly, claim 14 is not anticipated and is patentable under 35 U.S.C. §102(b) over Hebert.

Independent claims 16 and 21 teach the same elements and limitations of claim 1 that distinguish the claim over Hebert and are therefore allowable for the same reasons as claim 1.

Independent claim 32 requires a package having a recess. A planar bare die electronic device is disposed in the recess. A planarizing material fills the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In contrast, Hebert discloses that upon completion of the electrical connections, die-to-tape, and tape-to-contact fingers, the assembly with the housing may be protected by an encapsulent 41, extending up to the top of wall 11a (see Hebert at fig. 5 and col. 3, lines 7-14. Hence, the encapsulent 41 in Hebert does not create a level plane that includes the top of the chip (device), as required by claim 32. Planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Hebert. Accordingly, claim 32 is not anticipated under 35 U.S.C. §102(b) by Hebert. . Thus, claims 1, 14, 16, 21, and 32 are patentable over Hebert.

35 U.S.C. §103

Claim 4 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Wyland or Suzuki or Andros or Corisis or Hernandez or Hebert in view of Yoshida et al

(hereinafter Yoshida) (JP 59145537) or Oji et al. (hereinafter Oji) (JP 58197857). Claim 4, which is dependent on claim 1, requires a silicon package having a recess that includes a conductive region. The conductive region includes a first layer of titanium, a second layer of copper deposited on the first layer, and a third layer of chrome deposited on the second layer.

As described above, Wyland, Suzuki, Andros, Corisis, Hernandez and Hebert fail to disclose a package made of silicon having a recess into which a bare die electronic device is disposed. Furthermore, Wyland, Suzuki, Andros, Corisis, Hernandez and Hebert fail to disclose a recess that includes a conductive region having a first layer of titanium, a second layer of copper deposited on the first layer, and a third layer of chrome deposited on the second layer. In particular, Wyland discloses bonding wires 33 (see Wyland at fig. 1); Suzuki discloses bonding wire 9 and wiring pattern 3, of, for example, copper foil (see Suzuki at fig. 1 and col. 4, line29-30); Andros discloses conductive wire 49 made of aluminum or gold (see Andros at col. 5, lines 18-19) and connective metal such as copper (see Andros at col. 3, lines 9-11); Corisis discloses wire bonds 50 (see Corisis at col. 4); Hernandez discloses wire bonds 88 (see Corisis at fig. 1); and Hebert discloses wire bonds 29 and conductive tape that includes a copper foil (see Hebert at fig. 5 and col. 2 at lines 64-68).

Both Yoshida and Oji disclose a semiconductor device having a conductive region. The conductive region includes a first layer of titanium, a second layer of copper deposited on the first layer, and a third layer of chrome deposited on the second layer.

The disclosures of Yoshida and Oji fail to satisfy the deficiencies of the Wyland, Suzuki, Andros, Corisis, Hernandez and Hebert references. Specifically, both Yoshida and Oji fail to teach or suggest a silicon package having a recess, as required by claim 4. A silicon package having a recess is neither taught nor suggested by any combination of the above cited references. Thus, claim 4 is not obvious under 35 U.S.C. §103 from Wyland or Suzuki or Andros or Corisis or Hernandez or Hebert in view of Yoshida et al (hereinafter Yoshida) (JP 59145537) or Oji et al. (hereinafter Oji) (JP 58197857) and is allowable.

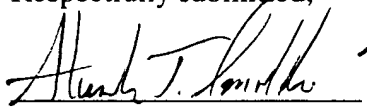
Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

It is believed that the application is now in order for allowance and Applicants respectfully request that a notice of allowance be issued. If any additional extensions are required, applicant hereby petitions for same and requests that any extension or other fee required for timely consideration of this application be charged to Deposit Account No. 19-4972.

If the Examiner has any questions as to the allowability of the currently pending claims or if there are any defects which need to be corrected, the Examiner is invited to speak to the Applicant's counsel at the telephone number given below.

DATE: February 15, 2002

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 2, 3, 7, 9, 14, 34, and 35 have been amended as follows:

2. An electronic component according to claim 1, wherein:

the conductive region is formed by metallization [metalization].

3. An electronic component according to claim 2, wherein:

the metallization [metalization] is achieved through a deposition process.

7. An electronic component according to claim 1, further comprising:

a plurality of metallized [metalized] bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

9. An electronic component according to claim 1, wherein:

the [The] device is a vertical device and the bottom of the device is coupled to the package in the recess.

14. An electronic component comprising:

a package having a recess, the recess including a first deposition-processed conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region

and the top terminal is [mechanically] electrically coupled to a second deposition-processed conductive region, and wherein at least a portion of the first and second conductive regions are essentially planar.

34. An electronic component according to claim 32, further comprising:

a metallization [metalization] layer.

35. An electronic component according to claim 34, wherein:

the metallization [metalization] layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

In the specification:

Paragraph beginning at page 3, line 1 has been amended as follows:

Fig. 1 is a side view of an electronic component. The electronic component is formed by a silicon package 10 from a silicon wafer surrounding an electronic device 12, preferably a bare die semiconductor device. The silicon package 10 includes a recess 14 in which the electronic device 12 resides. The electronic device 12 in the embodiment shown is a two-terminal device, although other multi-terminal devices, including both vertical and planar devices, may be used. The electronic device shown is a vertical device having a top terminal 15 and a bottom terminal 16. In the recess of the package, a conductive region 17 exists. The conductive region 17 covers all or a portion of the recess 14 and extends to a portion of the top 18 of the silicon package 10. The bottom terminal 16 of the two-terminal electronic device is electrically coupled to the conductive region 17. In preferred embodiments the conductive region is formed from metals such as titanium, copper and chrome. The bottom terminal 16 of the electronic device is secured to the conductive region by a conductive epoxy or solder 19. The recess 14 is filled with dielectric material 20 that surrounds the electronic device 12. If the dielectric layer 20 covers the top terminal 15 of the electronic device 12, the dielectric 20 that resides above the top terminal 15 is removed through photolithography. Dielectric may

also be removed at a point where a solder contact for the bottom terminal is desired. A metallization [metalization] layer 22 is applied over the dielectric after the top terminal 15 of the electronic device 12 is exposed. The metallization [metalization] is deposited and patterned by standard methods to the desired routing including solder contact areas. In the shown embodiment, another layer of dielectric 25 resides on top of the metallization [metalization] layer 22 fully encasing the electronic device 12 and only leaving the contacts exposed. It should be understood by those of ordinary skill in the art that for certain electronic devices a second layer of dielectric may not be needed. The solder contacts 21 are then created and preferably reside in the same plane so that the completed electronic component may be easily flip mounted onto a circuit board. In the preferred embodiment, the electronic device is a diode. However, it should be understood to one of ordinary skill in the art that other semiconductor devices, integrated circuits, or other electronic devices may be placed within the silicon package. This process produces a Wafer Level Chip-Scale Package (WLCSP) using silicon as the package.

Paragraph beginning at page 7, line 1 has been amended as follows:

In Fig. 5 is shown a package 510 for a bare die planar electronic device 520 that has all terminals 540 on one side of the chip. In this embodiment, the terminals 540 of the device 520 are repositioned using the technique above. The device [bare die] 520 is placed into a recess 515 of the package 510 and is adhered to the package using an adhesive 530 to mechanically couple the bare die 520 and the package 510. Into the portion of the recess 515 that is not filled by the bare die is placed a planarizing dielectric material 550. The planarizing material 550 creates an essentially planar surface for applying a layer of metallization [metalization] 560 so that the terminals 540 of the bare die 520 may be repositioned. Once the terminals 540 are repositioned, a second layer of dielectric 570 is applied keeping only the positions of the final contacts exposed. At the desired position of the final contact a metal contact 580 or soldering bump is added. The electronic component 500 is electrically exposed only at the repositioned contact points 580 with the rest of the electronic device 520 shielded from electrical coupling by the package 510 or dielectric 570. In such a fashion, planar electronic devices having

terminals that are positioned too close together and are at such a small scale that the terminals cannot maintain their electrical independence when placed on a circuit board may be made effectively larger by repositioning the contacts on the top of the package. Similarly, the terminals can be repositioned in any configuration that is more convenient for the end user of the electronic components. Thus, utilizing wafer-level processing, a smaller device may be made to be compatible with the dimensional requirements of a circuit board for fabrication of a more complicated product or subassembly.